PHILIPS

PRODUCT

DATA

INTEGRATED CIRCUITS

MARCH 1969

# D.T.L.

# INTEGRATED CIRCUITS

FC Series of D.T.L. Integrated Circuits

| Description | TYPE NUMBER Rc | non Rc |
|---|---|---|
| Single 8 Input NAND Gate | FCH111 | FCH101 |
| Dual 4 Input NAND Gate | FCH131 | FCH121 |
| Triple 3-3-2 Input NAND Gate | FCH161 | FCH141 |
| Triple 3 Input NAND Gate | FCH171 | FCH151 |
| Quadruple 2 Input NAND Gate | FCH191 | FCH181 |
| Sextuple Inverter | FCH211 | FCH201 |
| Dual 3 Input Line Driver NAND Gate | FCH221 | |
| Dual 4 Input Line Driver NAND Gate | FCH231 | |
| Single 5 Bit Comparator | FCH281 | |
| Single 10 Bit Parity Checker | FCH291 | |
| Single 4 Bit Decoder | FCH301 | |
| JK Flip-Flop | FCJ101 | |
| D.C.-Coupled JK Master-Slave Flip-Flop | FCJ111 | |
| Dual JK Master-Slave Flip-Flop | FCJ121 | |
| Dual JK Master-Slave Flip-Flop | FCJ131 | |
| Single Asynchronous 10-Counter | FCJ141 | |
| Dual JK Master-Slave Flip-Flop | FCJ191 | |
| Single JK Master-Slave Flip-Flop | FCJ201 | |
| Dual JK Master-Slave Flip-Flop | FCJ211 | |
| Quadruple Latch Flip-Flop | FCJ221 | |
| Monostable Multivibrator | FCK101 | |
| Level Detector | FCL101 | |
| Single Decoder NIT Driver | FCL111 | |
| Triple Gate Input Expander | FCY101 | |

All types listed are from the FC Series Standard Temperature Range 0° to +75°C with Dual-in-Line Plastic Encapsulation. Data on the FC Series Extended Temperature Range −55° to +125°C is available upon request.

# PREFACE TO DATA OF INTEGRATED CIRCUITS

1. Type designation code.

   See section Type designation.

2. General introduction to data of integrated circuits.

   The published data have been set up in such a form as to provide a maximum of information required by the system designer. They cover the necessary information for a worst-case system design as well as some typical device characteristics in those instances where the actual margin over the worst case is of importance.

3. Quick reference data.

   The main properties for quick device identification.

4. Outline drawing and pin 1 identification.

   A dimensional outline drawing with pin numbering and other information relevant to the outline are presented.
   For the dual in-line package a notch at one short side is the only reference for the pin 1 location. Any possible moulding mark on the package body should not be confused with pin 1 identification.
   For the flat pack the pin 1 is indicated by a small projection on the pin 1 terminal and/or by a dot on the top side of the package.
   For metal can encapsulations a tab on the circumference of the can determines the pin 1 location according to the drawing.

5. Ratings

   Ratings are limiting conditions beyond which the serviceability may be impaired. The rating system used in the integrated circuit data sheets is the Absolute Maximum Rating System as defined by the International Electrotechnical Commission in its publication 134. For further details see section Rating systems, item 2.
   If the integrated circuits are used under the conditions given in the sections "Characteristics" and "Additional System Design Data", operation within these ratings is ensured.





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6. Characteristics.

Characteristics are measurable properties of the device. Information given in this section is in the form of limits and typical values under a specific set of operating conditions. The Characteristics define the performance of the device under normal operating conditions and are given as a basis for system design. A typical value represents the mean value of the parameter spread of the device in normal production. Typical values are given for information only and are not subject to any form of guarantee.

7. Derived data.

Derived data constitute information derived from the Characteristics to provide further assistance to the system designer.

8. Additional system design data.

Information in this section is given to provide additional aid to optimal system design in practical cases, where the individual operating conditions of the Characteristics do not directly apply. The Additional System Design Data are derived from the Characteristics, partly supplemented by information based on calculations or particular additional measurements on a large quantity of production devices.
Though a 100% protection by measurement may not be ensured for all data in this section, this information can be used with a high degree of confidence for equipment design. In this manner various defined worst-case system conditions of loading, temperatures and supply voltages are taken into account.
The information is provided in the form of maximum, minimum or typical values.

9. Protection of the data.

Next to a severe in-line process and product quality control resulting in a high-built-in reliability, extensive electrical tests are applied to the semi-finished and the finished product to protect the data given.
Most of the data under the heading Characteristics are protected by 100% testing.

10. Logic drawing symbols.

For graphic logic symbols the system MIL STD 806B is used.
To assist the system designer in considering printed circuit board lay-out problems, drawings are added which indicate the logic configuration and the pin location of the device.

11. Letter symbols for digital circuits.

See section Letter symbols.

# LETTER SYMBOLS
# FOR DIGITAL INTEGRATED CIRCUITS

## 1. General.

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device and the function of the pertinent signal.
In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

The durations of signals and transients are unambiguously indicated by Signal HIGH and Signal LOW duration and by Rise and Fall time.

## 2. Terminal designations.

E = expander input (if necessary, this letter may be followed by one of the following input letters, e.g. EG = gate expander input)
G = gate input
J, K = condition inputs of JK flip-flop
N = negative supply
P = positive supply
Q = output
S = direct-set input
T = trigger (or toggle) input
Ø = common supply return and voltage reference

## 3. Subscript sequence for voltages and currents.

First subscript : terminal designation letter.
Second subscript: H (for HIGH) or L (for LOW), if applicable.
Third subscript : min or max, if applicable.
Examples: $V_P$, $I_{QL}$, $V_{QHmin}$

## 4. Polarity of current and voltage.

A current is defined to be positive when its conventional direction of flow is into the device.
Unless otherwise specified, a voltage is measured with respect to the reference terminal (Ø). Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

5 Time designations.

$t_d$ = delay time (average of $t_{dr}$ and $t_{df}$)

$t_{df}$ = fall delay time (Fig.3)

$t_{dr}$ = rise delay time (Fig.3)

$t_f$ = fall time (transition from HIGH to LOW, see Fig.1)

$t_H$ = signal HIGH duration (Fig.1)

$t_L$ = signal LOW duration (Fig.1)

$t_{pd}$ = propagation delay time (average of $t_{pdr}$ and $t_{pdf}$)

$t_{pdf}$ = fall propagation delay time (output falling, see Fig.2)

$t_{pdr}$ = rise propagation delay time (output falling, see Fig.2)

$t_r$ = rise time (transition from LOW to HIGH, see Fig.1)

$V_{pd}$ = reference voltage level for propagation delay

Fig.1

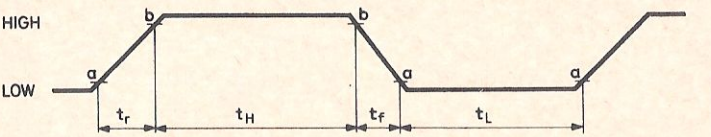



Fig.2

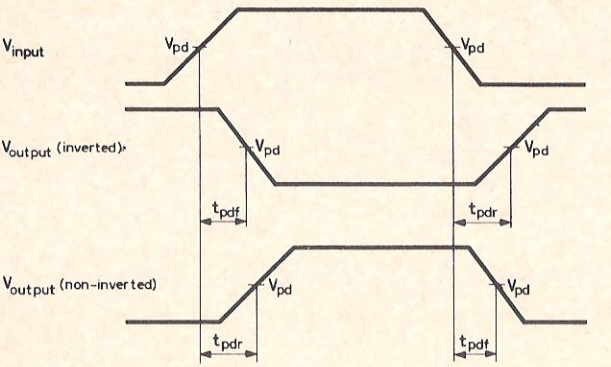
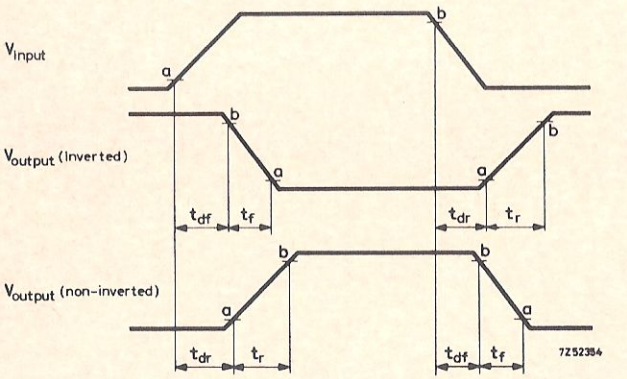



Fig.3




NOTE: a, b and $V_{pd}$ are specified voltage levels.

7Z3 1619

6. Other designations:

$M_L$ = d.c. noise margin, signal level LOW

$M_H$ = d.c. noise margin, signal level HIGH

$N_a$ = available d.c. fan-out (a guaranteed minimum)

P = power consumption, defined as the product of the supply current(s) and of the correponding supply voltage(s)

$P_d$ = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account

$T_{amb}$ = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction

$T_{stg}$ = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored

$V_{GL}$ = LOW threshold voltage, i.e. the LOW state voltage applied to the G input, at which for an inverting gate the output voltage does not drop below the specified limit $V_{QHmin}$ at a specified output current $I_{QH}$

$V_{GH}$ = HIGH threshold voltage, i.e. the HIGH state voltage applied to the G input, at which for an inverting gate the output voltage does not exceed the specified limit $V_{QLmax}$ at a specified output current $I_{QL}$

$\Delta V_Q$ = change of output voltage caused by a specified change of output current

## DIODE-TRANSISTOR LOGIC

### FC FAMILY

Medium speed, high fan-out, and an exceptionally high noise margin, make the FC family ideal for small computing, telecommunications, instrumentation, and control purposes. At 31 ns the stage delay is eminently suited to many civil and military applications, and where the higher speeds of TTL and $E^2CL$ are not demanded, DTL offers the advantages of system simplicity.

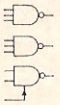
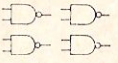
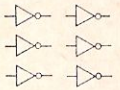
With over 30 circuits, including higher order functions, to choose from, the FC family provides system designers with the means to optimum system efficiency. The availability of all gates in a choice of versions—either with or without collector resistor, ensures that the cost and the power demands of a system can be significantly reduced by using wired-OR logic.

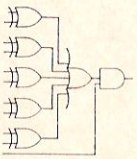
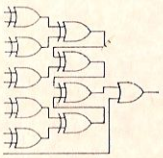
Noteworthy feature of this family is the special level-shifting diode that accounts for the exceptionally high noise margin.

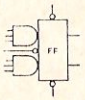
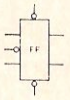
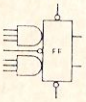
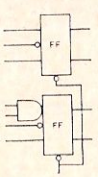
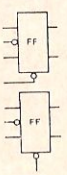
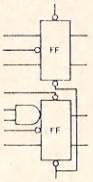
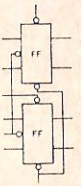
GENERAL DATA OF FC FAMILY (at 25°C)

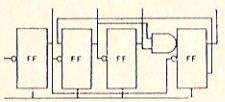
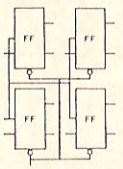
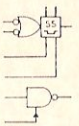
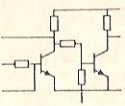
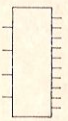
| | Operating temperature range |
|---|---|
| | Standard |
| Last figure of type number | 1 |
| Supply voltage | + 6V ± 5% |
| Propagation delay of gates | 31 ns |
| Clock frequency of flip-flops | 3 to 10 MHz |
| Operating ambient temperature | 0 to + 75 °C |
| Storage temperature | −35 to + 125 °C |
| Package | XG14 Dual in line |

## LETTER SYMBOLS AND SURVEY OF FC FAMILY (data at 25°C)

| Description (for positive logic) | | Single NAND gate | Dual NAND gate | Triple NAND gate | | Quadruple NAND gate | Sextuple NAND gate | Triple gate input expander |
|---|---|---|---|---|---|---|---|---|
| Symbol | | | |  | |  |  | |
| Type No. | without $r_e$ | FCH101 | FCH121 | FCH141 | FCH151 | FCH181 | FCH201 | FCY101 |
| | with $r_e$ | FCH111 | FCH131 | FCH161 | FCH171 | FCH191 | FCH211 | |

| Description (for postive logic) | Dual line driver NAND gate | | Single 5 bit comparator | Single 10 bit parity checker | Gated 4 bit decoder |
|---|---|---|---|---|---|
| Symbol | | |  |  | |
| Type number | FCH221 | FCH231 | FCH281 | FCH291 | FCH301[1]) |
| Available fan-out | 14 | 20 | 7 | 7 | 8 |
| Power consumption (per logic function) | 11 mW | 11 mW | 50 mW | 50 mW | 250 mW |
| Propagation Delay | 35 ns | 35 ns | 150 ns | 150 ns | 70 ns |

| Description | Single JK flip-flop | Single JK master-slave flip-flop | | Dual JK master-slave flip-flop | | | |
|---|---|---|---|---|---|---|---|
| Symbol |  |  |  |  |  |  |  |
| Type number | FCJ101 | FCJ111 | FCJ201 | FCJ121 | FCJ131 | FCJ191 | FCJ211 |
| Available fan-out | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Power consumption (per logic function) | 36 mW | 67 mW | 67 mW | 50 mW | 50 mW | 50 mW | 50 mW |
| Maximum clock rate | 10 MHz | 5 MHz | 5 MHz | 7 MHz | 7 MHz | 7 MHz | 7 MHz |

| Description | Single asynchronous counter | Quadruple latch flip-flop | Monostable multivibrator | Level detector | Single[2] decoder/ NIT driver |
|---|---|---|---|---|---|
| Symbol |  |  |  |  |  |
| Type number | FCJ141 | FCJ221 | FCK101[1] | FCL101 | FCL111 |
| Available fan-out | 6 | 8 | 8 | 3 | |
| Power consumption | 200 mW | 200 mW | 110 mW | 12 mW | 190 mW |
| Maximum clock rate | 5 MHz | 5 MHz | 2.5 MHz | 3.0 MHz | |

1) Available in flat package $\frac{1}{4}'' \times \frac{1}{4}''$ with type numbers FCK101Q.
2) NIT = Numerical Indicator Tube

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